What is claimed is:

1. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plural circuit cells, a switch for performing switching between the supply and non-supply of the first potential to each of semiconductor substrate areas of the plural circuit cells, a second wiring for supplying a signal for controlling the operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plural circuit cells; and

(b) invalidating the function of the switch and connecting the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plural circuit cells is fixed to the power supply potential.

2. The method according to claim 1, wherein the respective semiconductor substrate areas of the plural circuit cells include a semiconductor substrate area of first conductivity type, and a semiconductor substrate area of second conductivity type opposite to the first

conductivity type, the switch has a p channel type field effect transistor and an n channel type field effect transistor, the second wiring has a second wiring for the p channel type field effect transistor and a second wiring for the n channel type field effect transistor, and the third wiring includes wirings for the first conductivity type semiconductor substrate area and the second conductivity type semiconductor substrate area.

3. The method according to claim 1, wherein the second wiring and the third wiring, and the first wiring are connected within an internal circuit area.

4. The method according to claim 1, wherein the second wiring and the third wiring, and the first wiring are connected within a peripheral circuit area.

5. The method according to claim 1, wherein the plural circuit cells are formed with memory cells and logic gates or input/output circuits.

6. The method according to claim 1, further comprising a step of separating the second and third wirings from each other by a first circuit cell group that needs not supply the third potential, of the plural circuit cells, and a second circuit cell group that needs supply the third potential, of the plural circuit cells,

wherein said (b) step is effected on the second and third wirings connected to the first circuit cell group.

7. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plural circuit cells, a switch for performing switching between the supply and non-supply of the first potential to each of semiconductor substrate areas of the plural circuit cells, a second wiring supplying a signal for controlling the operation of the switch and having a portion intersecting the first wiring, and a third wiring supplying the first potential or a third potential higher than the first potential, and having a portion intersecting the first wiring and being connected to each of the semiconductor substrate areas of the plural circuit cells; and

(b) invalidating the function of the switch, and connecting the second wiring to the first wiring at the point intersecting the first wiring and connecting the third wiring to the first wiring at the point intersecting the first wiring, such that the potential supplied to each of the semiconductor substrate areas of the plural circuit cells is fixed to the power supply potential.

8. The method according to claim 7, wherein the second wiring and the third wiring, and the first wiring are connected within an internal circuit area.

9. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing design data of the semiconductor device having an internal circuit area, a plurality of circuit cells disposed in the internal circuit area, a first wiring for supplying a first potential corresponding to a power supply potential to the plural circuit cells, a first switch for performing switching between the supply and non-supply of the first potential to each of semiconductor substrate areas of the plural circuit cells, a plurality of input/output circuit cells disposed around the internal circuit area, a second switch disposed in each of the plural input/output circuit cells and for performing switching between the supply and non-supply of the first potential to each of semiconductor substrate areas of the input/output circuit cells, a second wiring for supplying a signal for controlling the operation of each of the first and second switches, and a third wiring supplying the first potential or a third potential higher than the first potential and connected to each of the semiconductor substrate areas of the plural circuit cells and the

plural input/output circuit cells; and

(b) invalidating the functions of the first and second switches, and connecting the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plural circuit cells and the plural input/output circuit cells is fixed to the power supply potential.

10. The method according to claim 9, wherein the second wiring and the third wiring, and the first wiring are connected within a peripheral circuit area.

11. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plural circuit cells, a switch for performing switching between the supply and non-supply of the first potential to each of semiconductor substrate areas of the plural circuit cells, a second wiring for supplying a signal for controlling the operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plural circuit cells;

(b) separating the second and third wirings from

each other by a first circuit cell group that needs not supply the third potential, of the plural circuit cells, and a second circuit cell group that needs supply the third potential, of the plural circuit cells; and

(c) invalidating the function of the switch with respect to the first circuit cell group, and connecting the second wiring and the third wiring connected to the first circuit cell group to the first wiring such that the potential supplied to each of semiconductor substrate areas of the first circuit cell group is fixed to the power supply potential.

12. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing design data of the semiconductor device having a plurality of field effect transistors, a first wiring for supplying a first potential corresponding to a power supply potential to the plural field effect transistors, a switch for performing switching between the supply and non-supply of the first potential to each of semiconductor substrate areas of the plural field effect transistors, a second wiring for supplying a signal for controlling the operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plural field effect transistors;

(b) separating the second and third wirings from each other by a first field effect transistor group that needs not supply the third potential, of the plural field effect transistors, and a second field effect transistor group that needs supply the third potential, of the plural field effect transistors; and

(c) invalidating the function of the switch with respect to the first field effect transistor group, and connecting the second wiring and the third wiring connected to the first field effect transistor group to the first wiring such that the potential supplied to each of semiconductor substrate areas of the first field effect transistor group is fixed to the power supply potential.

13. The method according to claim 12, wherein the second field effect transistor group is lower in threshold value than the first field effect transistor group.

14. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit cells, a first wiring for supplying a first potential corresponding to a power supply potential to the plural circuit cells, a switch for performing switching between the supply and

non-supply of the first potential to each of semiconductor substrate areas of the plural circuit cells, a second wiring for supplying a signal for controlling the operation of the switch, and a third wiring for supplying the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plural circuit cells; and

(b) invalidating the function of the switch, and disposing, instead of the switch, a connecting cell having information for connecting the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plural circuit cells is fixed to the power supply potential.

15. The method according to claim 14, wherein the connecting cell is disposed within an internal circuit area.

16. A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing design data of the semiconductor device having a plurality of circuit portions, a plurality of power supply switches respectively connected to the plural circuit portions and for respectively performing switching between the supply and non-supply of a power supply potential to the circuit portions, and

power supply switch control means for controlling the operations of the plural power supply switches;

(b) separating the power supply switch connected to the always operation-desired circuit portion of the plural circuit portions from the power supply switch control means; and

(c) fixing the input of the power supply switch connected to the always operation-desired circuit portion to the power supply potential.

17. A semiconductor device comprising:

(a) a plurality of circuit cells;

(b) a first wiring which supplies a first potential corresponding to a power supply potential to each of the plural circuit cells;

(c) a switch which performs switching between the supply and non-supply of the first potential to each of semiconductor substrate areas of the plural circuit cells;

(d) a second wiring which supplies a signal for controlling the operation of the switch;

(e) a third wiring which supplies the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plural circuit cells;

(f) a first circuit cell group corresponding to the plural circuit cells and that needs not supply the third

potential;

(g) the second wiring for the first circuit cell group;

(h) the third wiring for the first circuit cell group;

(i) a second circuit cell group corresponding to the plural circuit cells and that needs the supply of the third potential;

(j) the second wiring for the second circuit cell group;

(k) the third wiring for the second circuit cell group; and

(l) a connecting portion which invalidates the function of the switch with respect to the first circuit cell group, and connects the second wiring and the third wiring for the first circuit cell group to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the first circuit cell group is fixed to the power supply potential.

18. A semiconductor device comprising:

(a) a plurality of field effect transistors;

(b) a first wiring which supplies a first potential corresponding to a power supply potential to each of the plural field effect transistors;

(c) a switch which performs switching between the supply and non-supply of the first potential to each of

semiconductor substrate areas of the plural field effect transistors;

(d) a second wiring which supplies a signal for controlling the operation of the switch;

(e) a third wiring which supplies the first potential or a third potential higher than the first potential to each of the semiconductor substrate areas of the plural field effect transistors;

(f) a first field effect transistor group corresponding to the plural field effect transistors and that needs not supply the third potential;

(g) the second wiring for the first field effect transistor group;

(h) the third wiring for the first field effect transistor group;

(i) a second field effect transistor group corresponding to the plural field effect transistors and that needs the supply of the third potential;

(j) the second wiring for the second field effect transistor group;

(k) the third wiring for the second field effect transistor group; and

(l) a connecting portion which invalidates the function of the switch with respect to the first field effect transistor group, and connects the second wiring and the third wiring for the first field effect transistor group to the first wiring such that the

potential supplied to each of the semiconductor substrate areas of the first field effect transistor group is fixed to the power supply potential.

19. A semiconductor device comprising:

a plurality of circuit cells;

a first wiring which supplies a power supply potential to each of the plural circuit cells;

a power-feeding cell which supplies a potential to each of semiconductor substrate areas of the plural circuit cells;

a second wiring which supplies a signal for controlling the operation of the power-feeding cell; and

a third wiring which supplies the first potential to each of the semiconductor substrate areas of the plural circuit cells,

wherein the function of the power-feeding cell electrically connects the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plural circuit cells is fixed to the power supply potential.

20. The semiconductor device according to claim 19, wherein the second wiring and the third wiring, and the first wiring are connected within an internal circuit area.

21. The semiconductor device according to claim 19, wherein the second wiring and the third wiring, and the first wiring are connected within a peripheral circuit area.

22. A semiconductor device comprising:

a plurality of circuit cells;

a first wiring which supplies a power supply potential to each of the plural circuit cells;

a power-feeding cell which supplies a potential to each of semiconductor substrate areas of the plural circuit cells;

a second wiring supplying a signal for controlling the operation of the power-feeding cell and having a portion intersecting the first wiring; and

a third wiring supplying the first potential, having a portion intersecting the first wiring, and connected to each of the semiconductor substrate areas of the plural circuit cells,

wherein the function of the power-feeding cell electrically connects the second wiring to the first wiring at the point intersecting the first wiring and electrically connects the third wiring to the first wiring at the point intersecting the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plural circuit cells is fixed to

the power supply potential.

23. A semiconductor device comprising:

an internal circuit area;

a plurality of circuit cells disposed in the internal circuit area;

a first wiring which supplies a power supply potential to each of the plural circuit cells;

a first power-feeding cell which supplies a potential to each of semiconductor substrate areas of the plural circuit cells;

a plurality of input/output circuit cells disposed around the internal circuit area;

a second power-feeding cell disposed in each of the plural input/output circuit cells and for supplying a potential to each of semiconductor substrate areas of the input/output circuit cells;

a second wiring which supplies a signal for controlling the operation of each of the first and second power-feeding cells; and

a third wiring which supplies the first potential, said third wiring being connected to each of the semiconductor substrate areas of the plural circuit cells and the plural input/output circuit cells,

wherein the functions of the first and second power-feeding cells electrically connect the second wiring and the third wiring to the first wiring such that

the potential supplied to each of the semiconductor substrate areas of the plural circuit cells and the plural input/output circuit cells is fixed to the power supply potential.

24. A semiconductor device comprising:

a plurality of circuit cells;

a first wiring which supplies a power supply potential to each of the plural circuit cells;

a switch which performs switching between the supply and non-supply of a first potential to each of semiconductor substrate areas of the plural circuit cells;

a second wiring which supplies a signal for controlling the operation of the switch; and

a third wiring which supplies the first potential to each of the semiconductor substrate areas of the plural circuit cells,

wherein the second and third wirings are separated by a first circuit cell group that needs not supply the first potential, of the plural circuit cells, and a second circuit cell group that needs the supply of the first potential, of the plural circuit cells,

wherein the function of the switch with respect to the first circuit cell group electrically connects the second wiring and the third wiring connected to the first circuit cell group to the first wiring such that the

potential supplied to each of the semiconductor substrate areas of the first circuit cell group is fixed to the power supply potential.

25. A semiconductor device comprising:

a plurality of field effect transistors;

a first wiring which supplies a power supply potential to each of the plural field effect transistors;

a switch which performs switching between the supply and non-supply of a first potential to each of semiconductor substrate areas of the plural field effect transistors;

a second wiring which supplies a signal for controlling the operation of the switch; and

a third wiring which supplies the first potential to each of the semiconductor substrate areas of the plural field effect transistors,

wherein the second and third wirings are separated by a first field effect transistor group that needs not supply the first potential, of the plural field effect transistors, and a second field effect transistor group that needs the supply of the first potential, of the plural field effect transistors,

wherein the function of the switch with respect to the first field effect transistor group is invalidated, and the second wiring and the third wiring connected to the first field effect transistor group are connected to

the first wiring such that the potential supplied to each of the semiconductor substrate areas of the first field effect transistor group is fixed to the power supply potential.

26. A semiconductor device comprising:

a plurality of circuit cells;

a first wiring which supplies a power supply potential to each of the plural circuit cells;

a connecting cell which supplies a first potential to each of semiconductor substrate areas of the plural circuit cells;

a second wiring which supplies the first potential to the connecting cell; and

a third wiring which supplies the first potential to each of the semiconductor substrate areas of the plural circuit cells,

wherein the connecting cell connects the second wiring and the third wiring to the first wiring such that the potential supplied to each of the semiconductor substrate areas of the plural circuit cells is fixed to the power supply potential.

27. A semiconductor device comprising:

a plurality of circuit portions;

a plurality of power supply switches which are respectively connected to the plural circuit portions and

respectively perform switching between the supply and non-supply of a power supply potential to the circuit portions; and

power supply switch control means which control the operations of the plural power supply switches;

wherein the power supply switch connected to the always operation-desired circuit portion of the plural circuit portions is separated from the power supply switch control means, and

wherein the input of the power supply switch connected to the always operation-desired circuit portion is fixed to the power supply potential.